42.(New) The method according to claim 41, wherein said conformal insulating layer is an oxide layer is formed in a thermal process..--

REMARKS

These remarks are in response to the Office Action mailed on October 4, 2000, and for which a one-month extension is hereby requested. In that Office Action, claims 26-30 were allowed, claims 4-7 were objected to, and claims1-3 and 8-25 were rejected. Claim 4 has been rewritten in independent form, thereby conforming to the comments of the Office Action, and claims 4-7 should now be allowable. Claim 3 has also been rewritten in independent form and claims 1and 2 have been amended. These and the other rejected claims are believed allowable and are discussed below in two groups, claims 13-25 and claims 1-3 and 8-12. New claims 31-42 have been added and will be briefly discussed after the rejected claims.

The specification has also been amended to correct the informalities noted in the Office Action. The applicants thank the Examiner for noting these. Concerning the sentence beginning on page 14, line 19, although the sentence is believed comprehensible, it was not particularly well written. It has been rewritten in form, but introduces no new matter in substance.

Claims 13-25

Claims 13-18, 21, and 25 have been rejected under 35 U.S.C. 102(a) as being anticipated by Japanese patent application JP 11307722 of Watanabe, published on November 5, 1999. Claims 19, 20, and 22-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over either Watanabe alone or Watanabe in view of a secondary reference.

35 U.S.C. 102 states:

> A person shall be entitled to a patent unless-
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

As shown on its cover page in field (43), the Watanabe application was published on November 5, 1999. The present application was filed on July 12, 1999, prior to Watanabe's publication date. Consequently, the Watanabe application is not applicable as prior art against the present application. Therefore, claims 13-25 are believed allowable.

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Claims 1-3 and 8-12

Claims 1-3, 8, and 12 were rejected under 35 U.S.C. 102(e) as being anticipated by Nishihori et al., U.S. patent number 5,929,473. The Office Action indentifies the inter-level insulating film 36 if Nishihori et al.'s Figure 11c with the "conformal insulating layer" of claim 1. This layer 36 is the standard prior art thick, inter-metal insulation, such as described in the application on page 5, lines 7-9, that is formed after the lower electrode/gate layer has been etched, as shown in Figures 11a and 11b of Nishihori et al.

In contrast, the "conformal insulating layer" of claim 1 is formed prior to the lower etching process of steps 11-14 on page 3, lines 14-17, or on page 9, lines 17-20, of the application, and not afterwards these steps. As described in the present application on page 12, lines 1-18, the insulating layer of claim 1 is thin layer used to fill in the undercut 180 of Figure 3 of the application. Forming this layer is step 10a of the "Capacitor Process Module" of the flow on page 9 of the application, while the inter-level insulating film of Nishihori et al. would be part of the "subsequent steps" of step 14. Additionally, the insulating layer of claim 1 is a thin layer so as to not significantly degrade the photolithographic process established for when the capacitor process module is absent, while the inter-level insulating film 36 of Nishihori et al. as found in the prior art is a thick layer. The inter-level insulating film is to insure electrical isolation and its particular thickness is generally not particularly important, as long as it is sufficiently thick to provide this insulation.

This distinction is believed to be inherent in the original form of claim 1 through the language "*conformal* insulating layer"(emphasis added), as the inter-level insulating film 36 is not such a conformal layer. Consequently, claim 1 is believed allowable in its original form. However, to make the distinction over the prior art more explicit, claim 1 has been amended to include the step of "subsequently etching said bottom electrode layer" in order to make clear that the "insulating layer" of claim 1 is not the sort of inter-level insulating film of Nishihori et al., which occurs after the bottom electrode layer is etched. Therefore, it is respectfully submitted that claim 1 and its dependent claims, claims 2 and 12, are allowable. Claim 2 have been amended to accommodate the change to claim 1.

Claim 3 has been rewritten in independent form. It is respectfully submitted that Office Action's rejection of claim 3 is not well founded. The Office Action states:

> In regard to claims 3 and 8, Nishihori et al. uses examples of a non-insulating layer of Au (columns 8 and 9, lines 2 and 47 respectively). By virtue of being a metal one of its physical properties inherently would classify it as an anti-reflective layer or an anti-reflective coating.

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The Office Action is correct that gold is a non-insulating layer. However, it is respectfully submitted to in error that it is an anti-reflective layer. Being an anti-reflective layer is not an inherent property of a metal. An anti-reflective layer (ARL) is described in the application, for example, on page 1, line 3, to page 2, line 2:

> The ARL is an additional step included as part of the photolithographic process. It is a highly absorbing film formed directly on the substrate and upon which the photoresist then is formed. The ARL absorbs most of the radiation that penetrates the resist, generally in the 70-85% range.

These are not inherent properties of metals in general and of gold in particular.

Additionally, aside from not being anti-reflective, gold would not be used at this point in the formation of an integrated circuit. Gold is not used in silicon applications as it would be highly detrimental to device operation and is used in Nishihori only as a wiring layer (see, for example, column 9, lines 46-50). This is even noted in Nishihori at column 2, lines 62-67: "Precious metals, such as gold and platinum, have an excellent oxidation resistance. However, these materials are not appropriate for an IC...". Therefore, for any of these reasons, it is respectfully submitted that claim 3 and its dependent claims, claims 8-11, are therefore allowable.

Claim 9 is also rejected under 35 U.S.C. 103(a) over the single reference of Nishihori et al. This is also respectfully submitted to be in error. Nishihori et al. employs titanium nitride as an electrode. Although an ARL is non-insulating, as is the case with gold above, it does not follow that a material used as a conductor is suitable as an ARL.

New Claim and Conclusions

Claims 31-42 have been added and all relate to the embodiment found in the flow of page 9, lines 3-20, of the present application. As with original claim 4, new claims 31-35 are drawn to the feature that conformal layer is thin. As with claim 1 in its amended form, claims 36-39 highlight that the lower electrode is etched after insulating layer is formed. Claims 40-42 are drawn to the feature that the flow is designed so that the capacitor module is removable.

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For any of these reasons, reconsideration of the Office Action's rejection of claims 1-3 and 8-25, and consideration of new claims 31-42, is therefore respectfully requested, and an early indication of their allowability is earnestly solicited.

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Respectfully submitted,

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